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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Charles A Johnson  
Unisys Corporation  
Law Department M S 4773  
2470 Highcrest Road  
Roseville, MN 55113

EXAMINER

VITAL, PIERRE M

ART UNIT

PAPER NUMBER

2188

DATE MAILED: 03/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/651,597

Applicant(s)

ENGLIN ET AL.

Examiner

Pierre M. Vital

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 10 February 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 August 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

***Response to Amendment***

1. This Office Action is in response to applicant's communication filed February 10, 2003 in response to PTO Office Action mailed November 1, 2002. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.
2. Claims 1-20 have been presented for examination in this application. In response to the last Office Action, claims 1, 3-10, and 13-17 have been amended. No claims have been canceled or added. As a result, claims 1-20 are now pending in this application.
3. The objection to the specification has been withdrawn due to the amendment filed February 10, 2003.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting

directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1, 5, 6 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Duncan et al (US6,353,877).

As per claims 1 and 6, Duncan discloses a data processing system having a system bus {*Fig. 2, bus 20*} and having a processor with a level one cache memory {*i.e., primary cache*} responsively coupled to a level two cache memory {*processor chip 40 includes a secondary cache 48 (i.e., level two cache) on-chip*} which is responsively coupled to a level three memory {*Fig. 2, B-cache 52*} [col. 6, line 21-30]; said level two cache memory having cache storage {*Fig. 2, data store 46*} and tag storage {*Fig. 2, duplicate tag store 54*}, and having a circuit for SNOOPing said system bus [col. 7, lines 20-25], the improvement comprising a first dedicated path between said system bus and said cache storage {*Fig. 2, processor chip 40 has direct path to bus 20*} and a second dedicated path between said system bus and said tag storage {*Fig. 2, duplicate tag store 54 has direct path to bus 20*}.

As per claim 5, Duncan discloses a data processing system comprising a level three cache memory [col. 6, lines 28-31].

As per claim 11, Duncan discloses the claimed invention as detailed per claim 1 above. Duncan further discloses formulating a SNOOP request [col. 7, lines 22-25]; presenting said SNOOP request on said system memory bus to said level two cache

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memory {i.e., all devices coupled to system bus snoops the bus, including secondary cache} [col. 8, lines 10-12]; routing said SNOOP request directly to said tag memory {address presented to duplicate tag store} [col. 8, lines 10-14]; processing said SNOOP request [col. 8, lines 14-20].

### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 2-4, 8, 10, 12 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duncan et al (US6,353,877) and Stevens et al. (US5,426,765).

As per claims 2 and 12, Duncan discloses the claimed invention as detailed above in the previous paragraphs. However, Duncan does not specifically teach a control logic which provides the highest priority for a SNOOPing as recited in the claims.

Stevens et al. disclose a control logic which provides the highest priority for a SNOOPing [col. 4, lines 23-32].

It would have been obvious to one of ordinary skill in the art, having the teachings of Duncan and Stevens et al. before him at the time the invention was made, to modify the system of Duncan to include a control logic which provides the highest

priority for a SNOOPing because it would have provided minimal effect on system speed by allowing the cache system to efficiently service its local processor while also guaranteeing access to all snoop requests on the host bus to maintain cache coherency [col.4, lines 15-20] as taught by Stevens et al.

As per claim 3, Duncan discloses a level two cache memory further comprising a duplicate tag memory {*Fig. 2, duplicate tag store 54*}.

As per claim 4, Duncan discloses a data processing system comprising a plurality of instruction processors [col. 6, lines 21-22].

As per claim 10, Duncan discloses a data processing system wherein a snoop request is responsively coupled to a duplicate tag memory [col. 8, lines 11-13].

As per claim 14, Duncan discloses routing said SNOOP request to a duplicate tag memory {*snoops the bus and present an address to the duplicate tag store*} [col. 8, lines 11-15].

As per claim 15, Duncan discloses processing said SNOOP request regarding said duplicate tag memory [col. 8, lines 11-20].

8. Claims 7, 9, 13 and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duncan et al (US6,353,877) and Stevens et al. (US5,426,765) and further in view of Fu (US6,457,087).

As per claim 7, the combination of Duncan and Stevens discloses the claimed invention as detailed above in the previous paragraphs. However, Duncan and Stevens

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do not specifically teach a data request transferred from said level one cache memory to a level two cache memory.

Fu discloses a data request transferred from said level one cache memory to a level two cache memory *{when cache miss occurs, the request is transferred to the next cache level as is well known in the art}* [col. 10, lines 4-7].

As per claim 16, the combination of Duncan and Stevens discloses the claimed invention as detailed above in the previous paragraphs. However, Duncan and Stevens do not specifically teach caching data in the next level when said data does not reside at the lower level cache.

Fu discloses caching data in the next level when said data does not reside at the lower level cache [col. 10, lines 38-48].

As per claims 9 and 13, the combination of Duncan and Stevens discloses the claimed invention as detailed above in the previous paragraphs. However, Duncan and Stevens do not specifically teach a data processing system comprising a level one tag memory located within a level one cache memory, a level two cache memory further comprising a duplicate tag memory which maintains a duplicate of information within said level one tag memory.

Fu discloses a data processing system comprising a level one tag memory located within a level one cache memory *{i.e., L1 tag memory 246}* [Fig. 5C], a level two cache memory further comprising a duplicate tag memory which maintains a duplicate of information within said level one tag memory *{i.e., L2 duplicate tag memory 234}* [Fig. 5A].

It would have been obvious to one of ordinary skill in the art, having the teachings of Duncan and Stevens and Fu before him at the time the invention was made, to modify the system of Duncan and Stevens to include a data request transferred from said level one cache memory to a level two cache memory; a data processing system comprising a level one tag memory located within a level one cache memory, a level two cache memory further comprising a duplicate tag memory which maintains a duplicate of information within said level one tag memory because it would have provided flow control of read and write transaction in the system by searching the caches for the intended data [col. 6, lines 38-48] and improved cache coherency in the system by allowing the snoop to initiate the appropriate actions to change the state of all the other duplicate tags in the system [col. 31, lines 11-16] as taught by Fu.

Claim 17 is rejected as per claims 2 and 12 above.

As per claim 18, Duncan discloses means responsively coupled to a level two caching means for bussing system memory data [col. 6, lines 24-27]; means responsively coupled to a bussing means for interfacing said bussing means directly to a storing means {Fig. 2, *duplicate store interfacing with bus 20*}; Stevens discloses means responsively coupled to said bussing means for interfacing said bussing means directly to said maintaining means [Fig. 2, *bus control logic 58 interfaces with bus 20*].

Claim 19 is rejected as per claims 9 and 13 above.

Claim 20 is rejected as per claim 10 above.



***Response to Arguments***

9. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9000.

*Puv*  
Pierre M. Vital  
March 13, 2003

*Reginald G. Bragdon*  
REGINALD G. BRAGDON  
PRIMARY EXAMINER